REMARKS

Claims 1-51 are pending in the present application. Claims 1-3, 6, 7, 9, 10, 12-14, 18, 19, 23, 24, 26, 30-39, and 41-51 are amended above. No new matter is added by the claim amendments. Entry is respectfully requested.

The specification stands objected to for various informalities stated in the Office Action. The specification is amended above in a manner consistent with suggestions provided in the Office Action. Entry of the amendments is respectfully requested.

1-44, 49, and 51 stand rejected under 35 U.S.C. 112, second paragraph, for reasons stated in the Office Action. The claims are amended above in a manner that is believed to overcome the rejections. Entry of the amendments and removal of the rejections are respectfully requested.

With regard to the rejection of claims 1, 12, 23, 24, and 41, the claims are amended to clarify that the "memory module" comprises the "first memory module". Both the "first memory module" and the "second memory module" can be used in the "memory system".

With regard to the rejection of claim 1, the claim is amended to clarify that the "second buffer" is part of the "first memory module".

With regard to the rejection of claim 4, the Applicant believes that this rejection was intended to apply to claim 6. Claim 6 is amended to state "memory device", which has an antecedent in claim 1.

With regard to the rejection of claim 6, the claim is amended to replace "the data signals" with "data signals", to clarify that the "data signals" being referred to are "data signals" that are exchanged between the memory device and the second buffer.

With regard to claim 42, the term "the second memory module" finds an antecedent in the last line of claim 41.

Claims 23, 24, 26, 30, 34, 35, 36, 37, 41, 42, 44, 45, 46, 49, 50 and 51 are rejected under 35 U.S.C. § 102 as being anticipated by Halbert, *et al.* (U.S. Patent No. 6,625,687). Claims 1-4, 6, 7, 9-15, 18-21, 27, 31-33, 38-40, 47 and 48 are rejected as being unpatentable over Halbert. in view of Gustavson, *et al.* (U.S. Patent No. 6,442,644 - hereinafter "Gustavson"). Claims 5 and 16 are rejected as being unpatentable over Halbert, *et al.* in view of Gustavson. and further in view of Johnson, *et al.* (U.S. Patent No. 5,987,576). Claim 28 is rejected as being unpatentable over Halbert, *et al.* in view of Johnson, *et al.*

Independent claims 1, 12, 23, 34, 41, 45, 46, 47, 48, 49, 50, and 51 are amended above to state that certain generated clock signals are generated "in response to, and in phase with" certain received clock signals.

For example, amended independent claim 1 states that a "second write clock signal" is generated "in response to, and in phase with, the first write clock signal". Also, the "memory write clock signal" is generated "in response to, and in phase with, the first write clock signal". Also, the "memory read clock signal" is generated "in response to, and in phase with, a memory write clock signal".

Amended independent claim 12 states that a "second write clock signal" is generated "in response to, and in phase with, the first write clock signal".

Amended independent claim 23 states that a "memory write clock signal" is generated "in response to, and in phase with, the first write clock signal".

Amended independent claim 34 states that a "memory read clock signal" is generated "in response to, and in phase with, a memory write clock signal". Also, the "memory write clock signal" is generated "in response to, and in phase with, the first write clock signal".

Amended independent claim 41 states that a "second read clock signal" is generated "in response to, and in phase with, the first write clock signal".

Amended independent claim 45 states that a "second write clock signal" is generated "in response to, and in phase with, the first write clock signal". Also the "memory write clock signal" is generated "in response to, and in phase with, the first write clock signal". Also the "memory read clock signal" is generated "in response to, and in phase with, the memory write clock signal".

Amended independent claim 46 states that a "second write clock signal" is generated "in response to, and in phase with, the first write clock signal". Also the "memory write clock signal" is generated "in response to, and in phase with, the first write clock signal". Also a "memory read clock signal" is generated "in response to, and in phase with, the memory write clock signal". Also the "second read clock signal" is generated "in response to, and in phase with, the first read clock signal".

Amended independent claim 47 states that a "second write clock signal" is generated "in response to, and in phase with, the first write clock signal". Also, the "memory write clock signal" is generated "in response to, and in phase with, the first write clock signal". Also, the "memory read clock signal" is generated "in response to, and in phase with, a memory write clock signal".

Amended independent claim 48 states that a "second write clock signal" is generated "in response to, and in phase with, the first write clock signal".

Amended independent claim 49 states that a "memory write clock signal" is generated "in response to, and in phase with, the first write clock signal".

Amended independent claim 50 states that a "memory write clock signal" is generated "in response to" and "in phase with" a "first write clock signal". Also, the "memory read clock signal" is generated "in response to, and in phase with, the memory write clock signal".

Amended independent claim 51 states that a "second read clock signal" is generated "in response to, and in phase with, the first write clock signal".

In this manner, the various clock signals that are generated "in response to" the certain stated source clock signals, are each generated to be "in phase with" the source clock signal. In other words the source signal and the generated signal have the same phase relationship. This eliminates the need for clock domain crossing within the memory module for those clock signals that are "in-phase", or "share the same phase relationship", simplifying the system clocking configuration, and leading to more stable and efficient data exchange throughout the memory system (see specification, page 14, line 14 - page 17, line 15).

It is respectfully submitted that neither Halbert nor Gustavson teach or suggest the present invention as claimed in amended independent claims 1, 12, 23, 34, 41, 45, 46, 47, 48, 49, 50, and 51. In particular, neither reference teaches or suggests generating the stated clock signals "in response to" and "in phase with" the received source clock signals. Halbert teaches the elements of a point-to-point memory system, but fails to discuss maintaining a phase relationship between clock signals, as claimed in the present inventions. Gustavson is cited as showing use of a first command buffer 301 and a second data buffer 302 in FIG. 3. However, Gustavson, like Halbert, fails to suggest maintaining a phase relationship between clock signals.

In view of the above, it is submitted that Halbert fails to anticipate the invention as claimed in amended independent claims 23, 34, 41, 45, 46, 49, 50 and 51. In addition, it is

submitted that the combination of Halbert and Gustavson fails to teach or suggest the invention as claimed in claims 1, 12, 47 and 48. Accordingly, reconsideration of the rejection and allowance of independent claims 1, 12, 23, 34, 41, 45, 46, 47, 48, 49, 50, and 51 are respectfully requested.

With regard to the various dependent claims, it follows that these claims should inherit the allowability of the independent claims from which they depend.

Closing Remarks

It is submitted that all claims are in condition for allowance, and such allowance is respectfully requested. If prosecution of the application can be expedited by a telephone conference, the Examiner is invited to call the undersigned at the number given below.

Respectfully submitted,

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Mills & Onello, LLP
Eleven Beacon Street, Suite 605
Boston, MA 02108
Telephone: (617) 994-4900, Ext. 4902
Facsimile: (617) 742-7774
J:\SAM\0211\amendmenta.wpd

Anthony P. Onello, Jr.
Registration Number 38,572
Attorney for Applicant